ATLAS CSC Preamp/Shaper Design Review
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P. O'Connor, A. Kandasamy, BNL

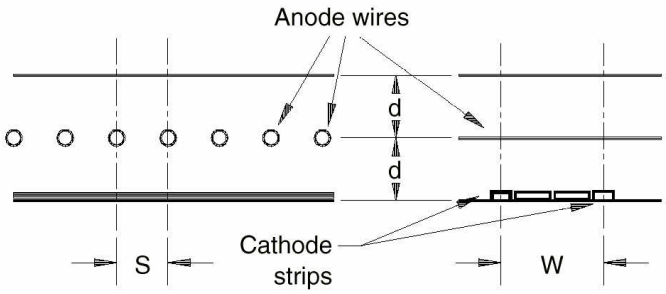
1. System Overview

1.1 ATLAS Cathode Strip Chambers

ATLAS CSC chambers form the first station of the endcap muon spectrometer for η between 2.0 and 2.7. Track position is found by interpolation using an accurate measurement of the charge induced on 3 adjacent strips.

Strip length	up to 1m
Strip pitch	5 mm
Anode-cathode spacing	2.5 mm
Gas gain	1.5 x 10^4 - 1pC
Anode charge	1 pC
Strip capacitance	20 - 50pF
Rate (including background)	150 kHz max per strip
Radiation dose	< 10 krad over 10 years

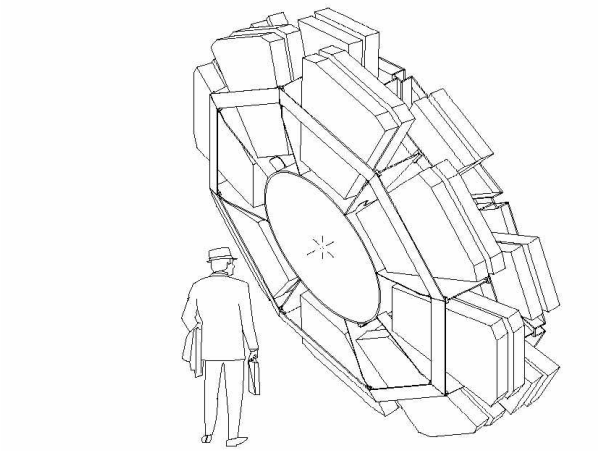
In each endcap the chambers are arranged in a wheel, as shown in the figure. Electronics will be located along the edges of the chambers on the 96-channel ASM boards. There are 32 chambers per endcap, with 8 ASM boards each.



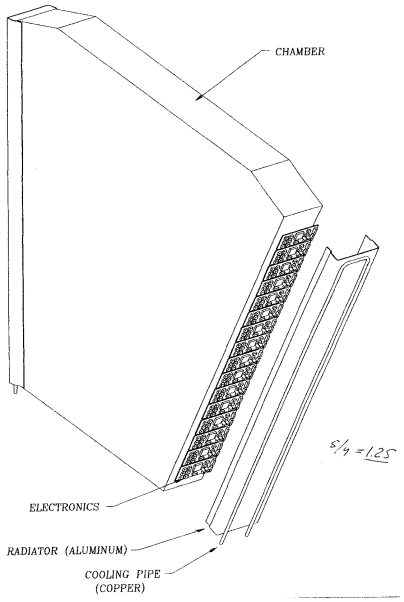
CSC Construction: S = 2.54 mm, d = 2.54 mm, W = 5.08 mm

1.2 Signal processing

The CSC preamp/shaper is an outgrowth of earlier work for the CSC system of the GEM detector at the SSC. In that chip each channel contained in addition to preamps and shapers, a fast discriminator, track and hold, and multiplexer. The rates and occupancies at the SSC were low, so a data-driven storage using track and hold stages was preferred for its economy and freedom from digital crosstalk. In ATLAS the rates are too high to support a deadtimeless track and hold architecture. The present preamp/shaper contains only amplifiers and their bias circuits. There are no digital signals of any kind on this first prototype; however, we may in the future add digital configuration switches which are not active during data taking.

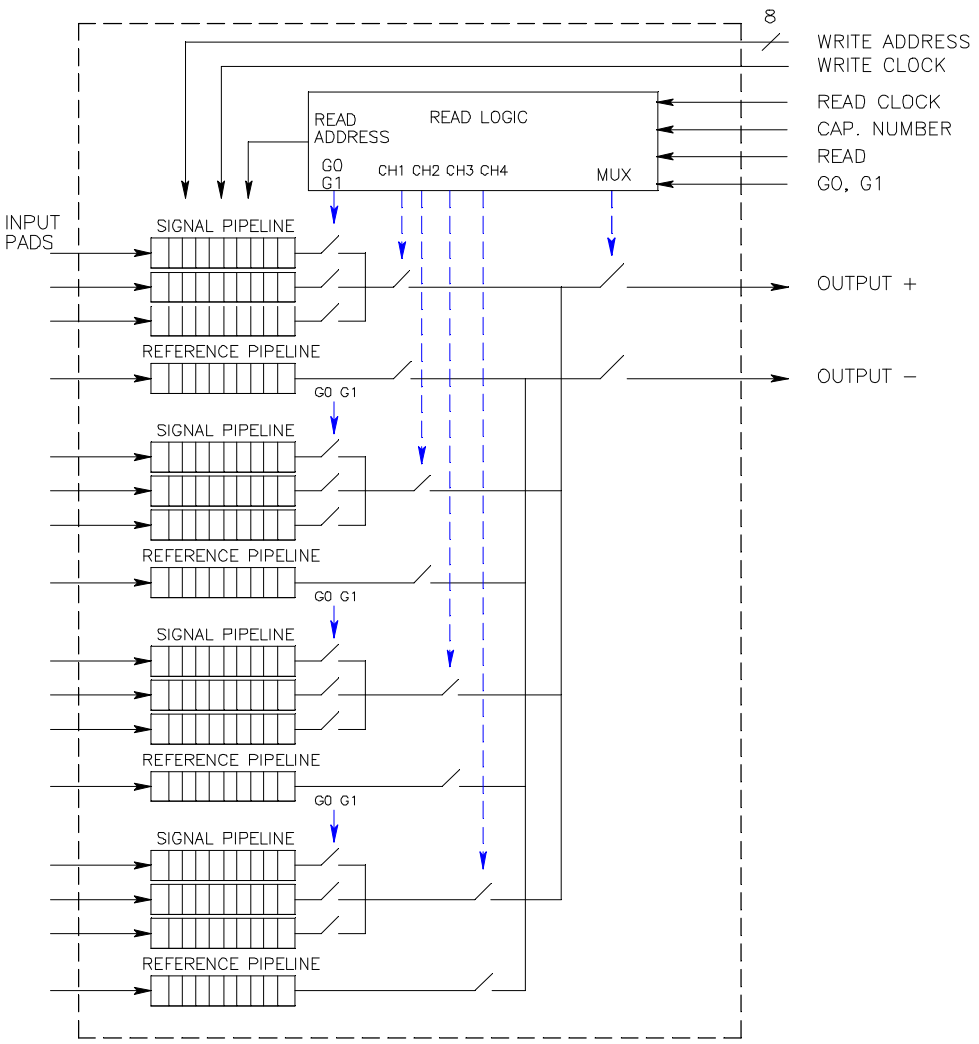


CSC Wheel Assembly



CSC Electronics Location on Chambers

In the LHC version the charge on a strip is processed by the preamp/shaper chip, then sent to a switched capacitor analog memory (SCA) for storage prior to digitization. Upon receipt of a trigger signal 3-5 samples of the waveform on each strip are digitized, and zero-suppressed data is transmitted off-detector via optical fiber link.



SCA Architecture

The preamp/shaper chip (subject of this review) is fabricated in 0.5 micron CMOS and operates off a 0-3.3V power supply. It has a conventional charge-sensitive preamplifier front end. The shaping is bipolar, with a high-order complex Gaussian shaper having a peaking time of around 70 nsec. The SCA is a 5V CMOS design by W. Sippach at Nevis Laboratories. Originally intended for the ATLAS Liquid Argon Calorimeter this chip has more than enough dynamic range and accuracy for use with the CSCs. The channel multiplexing architecture, originally arranged for storing signals from 4 channels of a tri-gain shaper, can be used for 12 single-gain CSC channels. A 10-bit ADC will be used for digitization at 5 – 10 MHz rate. The data rate from one ASM board will be of the order of 500 Mbits/sec before zero suppression.

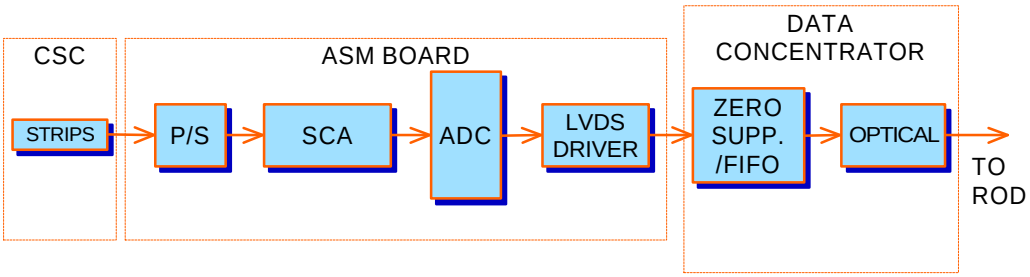
1.3 ASM Boards

The preamp/shaper, SCA, ADC, and necessary control logic will be mounted on 96-channel ASM boards along the edges of the chambers. The 13 x 24 cm boards are populated on both sides. A transition board is necessary to re-map the strips as they emerge from the CSC onto the input edge of the ASM boards. As

an option, the preamp/shapers may be mounted on this transition board to be closer to the strips and to achieve better isolation from the digital signals on the ASM board.

1.4 Other on-chamber electronics

After digitization, the signals are sent over short LVDS links to a Data Concentrator Card mounted on the large face of the chamber. There the signals are buffered and zero suppressed, reducing the data rate by about 1/10. Formatting and header information is inserted into the data stream at this point. Optical links carry the data to RODs located off-detector. A downstream optical link carries trigger and timing information to each CSC chamber.



CSC Signal Flow

2. Circuit Specifications

In an interpolating position-sensitive system the front end must have good signal-to-noise ratio, good linearity, and low crosstalk. Since we expect a high background the pulse shaping must be a compromise between low noise and low pileup. Beam test results show that crosstalk between channels degrades the position resolution and is difficult to correct in offline analysis.

Noise	< 2000 e-
Max. linear charge	300-400 fC
Pulse peaking time (5% - 100%)	70 nsec
FW1%M	430 nsec
Shape	bipolar
Crosstalk	< 0.5%

3. Circuit Design

3.1 Architecture

The SCA chip has one “reference” channel for every three “live” channels (see figure). The live and reference channels are presented to the output multiplexer, then subtracted to reject common-mode noise. In the preamp/shaper, rejection of common-mode pickup, power supply disturbances, and substrate noise is also important. However, a differential signal structure was rejected for the following reasons. First, the

input stage of the preamp requires high power (15 mW) and large area (5000/0.6 micron device.) Thus the pseudo-differential design of the U. Penn. ASD is prohibitive in terms of power and area. Secondly, the preamp/shaper has to interface to the SCA's unusual channel structure. If the preamp/shaper had differential output, we would have to either throw one phase away, use an external difference amp, or use two SCA channels for each signal. These alternatives are too costly. As a result, the preamp/shaper uses single-ended amplifiers to amplify the strip signals. One or several unused signal channels can be used to feed the reference channels of the SCA to improve the common-mode noise rejection. As mentioned in Section 1, there are no digital circuits on the prototype preamp/shaper chip.

3.2 Preamplifier

3.2.1 Input device noise optimization

The input device (M1 in schematic) is chosen to be an NMOS transistor with minimum channel length. Then, the width is selected to give minimum noise for the allotted power budget. Using the standard analysis the device width that minimizes series white noise is the one that gives a FET capacitance of CDet/3. However, in our case that puts the device well into the weak inversion region where the standard analysis is no longer valid. We reduce the device width to put it near the border of weak-strong inversion to achieve a lower capacitance at the same gm. Finally, a behavioral model in MathCAD is used to select the input device dimensions. The current source and cascode devices in the preamp are also chosen for low noise using this mode.

3.2.2 DC feedback and compensation

For our expected strip capacitance of 20 – 50 pF we choose a preamplifier feedback capacitance of 1.2 pF. A NMOS FET (M24 in schematic) biased in the triode region is used for to provide DC feedback with an equivalent resistance of about 1.2 MegOhm. This resistance gives negligible parallel noise and provides a reset time short enough to keep the preamp from saturating under the highest expected rate. The bias circuit for the feedback FET is found in the Bias circuit schematic. We form a replica circuit which allows us to set the feedback FET's gate potential with reference to the input/output potential of the amplifier; it is essential to use such a scheme which tracks temperature and process variation to prevent excessive variation of the effective RF.

The compensation circuit, M25 – C3, is a nonlinear version of the standard pole-zero compensation used in discrete designs. M25 and C3 are 4X scaled copies of M24 and C5. The compensation FET M25 sees the same gate, source, and drain voltage as the feedback FET and so the 2 devices maintain a constant resistance ratio even as the preamp output swings in response to a large transient signal. In practice the feedback FET nonlinearity is well-compensated by this system.

3.3 Shaper

3.3.1 Gaussian filter synthesis

The method of Ohkawa is used to design a 7^{th} order shaper which is the best approximation to a true Gaussian waveform. This technique gives normalized natural frequencies and Q factors of the first and second-order sections making up the filter as follows:

Stage	Order	ω0	Q
1	1	3.3802	-
2	2	3.4559	0.5234
3	2	3.7124	0.6098
4	2	4.2943	0.8549

For a 5%-100% peaking time of 70 nsec, the normalized frequency must be scaled by (1/105 nsec). The four sections are arranged in cascade in order of increasing Q. Three of the sections are lowpass, one is bandpass to achieve a bipolar shape. The bandpass section is put at the end so that its input-referred noise is kept low.

3.3.2 Second order sections

Each second-order section is made with a multiple feedback topology. This arrangement uses a high-gain inverting amplifier whose input serves as a virtual ground, and has low sensitivity to component tolerances.

3.3.3 Amplifier design

The amplifier stages used in the shaper are NMOS-input folded cascodes with followers. Simulations showed that the amplifiers don't unduly influence the transfer function if they have a gain-bandwidth product of >150 MHz and a DC gain of over 500. The amplifiers dissipate about 3 mW each. Small current sources at the inputs of each amplifiers allow the input and output DC levels to differ, where necessary to maintain high dynamic range. For each local loop, the loop gain was measured to insure that the phase margin was greater than 60°.

3.3.4 Noise sources in shaper

Several resistors in the shaper contribute non-negligible input-referred noise. The resistors R6, R10, and R12 contribute an input-referred noise of about 300, 500, and 280 rms electrons respectively. Their noise can be reduced by (1) increasing the preamp gain, (2) increasing the ratio between compensation and feedback capacitors, (3) increasing the feedback resistance of the compensation stage, or (4) reducing the value of the shaper resistors with consequent increase in capacitor value to retain the proper time constants. Solutions (1)-(3) reduce the dynamic range while with solution (4) the circuit area increases and the amplifiers must have higher current to drive the lower-impedance capacitors.

3.4 Output stage

The final stage is a symmetric OTA with rail-to-rail class AB output. Dissipating only 5 mW, this circuit can drive up to 100 pF capacitive loads to within 0.1V of either supply rail at slew rates of over 50 V/μsec. The Class AB control circuit uses a "floating current source" , MN1-MP1, to achieve a low quiescent current in the output transistors. The transient current can be up to 10X the quiescent current. This amplifier is internally compensated by the Miller capacitors CC1 and CC2. In a gain-of-2 configuration with a load capacitance of 50 pF, the phase margin is 35°.

3.5 Bias circuits

The majority of the bias currents are generated by means of a threshold-referenced current source which is insensitive to supply voltage variations. The current is defined by the ratio of a transistor threshold voltage V_T and a resistor R:

$$I_{bias} = \frac{V_T}{R}$$

Monte Carlo simulation with representative parameter variations for this process showed the bias currents so derived to vary less than 10% (1 signa) from their nominal values.

5. Design methodology

Monte Carlo simulations were performed using parameters determined from the last 18 MOSIS runs of the HP 0.5 micron CMOS process. We found the standard deviations of each parameter as follows:

Parameter		NMOS	PMOS
Tox	1.1%		
FET - VTH0		17 mV	49 mV
FET - U0		1.3%	3.7%
FET - WINT		.011 micron	.013 micron
FET - LINT		.009 micron	.009 micron
RESISTOR	3%		
CAPACITOR	2%		

The circuit was simulated using LOT variations of 3 sigma and DEVICE variation 0.3 sigma. The Monte Carlo runs used the uniform distribution.

In addition to Monte Carlo we simulated the circuit for variations in VDD, Cdet, and Cload.

Layout was done in Magic using generator scripts for the transistors, capacitors, and resistors. The most recent Submicron CMOS design rules from MOSIS, which include "antenna rules" for process-induced gate oxide damage, were used in MAGIC's on-line design rule checker. The circuit was checked by extracting the netlist from the layout and simulating it. We also performed an LVS check using Tanner tools to compare the schematic and layout-extracted netlists.